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June 30, 2005

Date

Kevin L. Daffer

APPLICATION NO.	FILING DATE	FIRST NAMES INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/846,119	04/30/2001	Yitzhak Gilboa	5298-04700	5235

TITLE OF INVENTION: METHOD OF MAKING A PLANARIZED SEMICONDUCTOR STRUCTURE

APP N TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1,400.00	\$0.00	\$1,400.00	07/08/2005
EXAMINER	ART UNIT	CLASS-SUBCLASS			
Goudreau, George A.	1763	438-700000			

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2 Mollie E. Lettang

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3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type) PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the PTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Cypress Semiconductor Corp.

(B) RESIDENCE (CITY & STATE OR COUNTRY): San Jose, CA

Please check the appropriate assignee category indicated below (will not be printed on the patent): ☐ individual ☒ corporation or other private group entity ☐ government

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☒ Issue Fee☐ Publication Fee☒ Advance Order - # of Copies 4

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(Authorized Signature)

Kevin L. Daffer
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Patent and Trademark Office U.S. DEPARTMENT OF COMMERCE

PAGE 1/1 * RCVD AT 6/30/2005 3:57:18 PM [Eastern Daylight Time] * SVR:USPTO-EFXXF-2/0 * DNIS:7464000 * CSID:512 703 1250 * DURATION (mm-ss):01:16

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